

4.5MHz, BiMOS Operational Amplifier with MOSFET Input/Bipolar Output

The CA3140A and CA3140 are integrated circuit operational amplifiers that combine the advantages of high voltage PMOS transistors with high voltage bipolar transistors on a single monolithic chip.

The CA3140A and CA3140 BiMOS operational amplifiers feature gate protected MOSFET (PMOS) transistors in the input circuit to provide very high input impedance, very low input current, and high speed performance. The CA3140A and CA3140 operate at supply voltage from 4V to 36V (either single or dual supply). These operational amplifiers are internally phase compensated to achieve stable operation in unity gain follower operation, and additionally, have access terminal for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS field effect transistors in the input stage results in common mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute for single supply applications. The output stage uses bipolar transistors and includes built-in protection against damage from load terminal short circuiting to either supply rail or to ground.

The CA3140A and CA3140 are intended for operation at supply voltages up to 36V ($\pm 18V$).

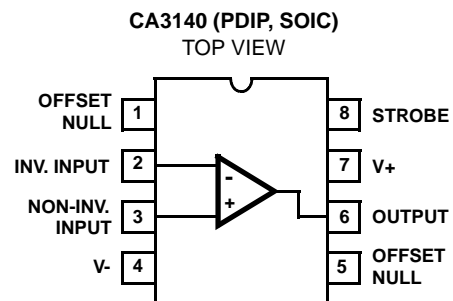
Features

- MOSFET Input Stage
 - Very High Input Impedance (Z_{IN}) -1.5T Ω (Typ)
 - Very Low Input Current (I_I) -10pA (Typ) at $\pm 15V$
 - Wide Common Mode Input Voltage Range (V_{ICR}) - Can be Swung 0.5V Below Negative Supply Voltage Rail
 - Output Swing Complements Input Common Mode Range
- Directly Replaces Industry Type 741 in Most Applications
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Ground-Referenced Single Supply Amplifiers in Automobile and Portable Instrumentation
- Sample and Hold Amplifiers
- Long Duration Timers/Multivibrators (μ seconds-Minutes-Hours)
- Photocurrent Instrumentation
- Peak Detectors
- Active Filters
- Comparators
- Interface in 5V TTL Systems and Other Low Supply Voltage Systems
- All Standard Operational Amplifier Applications
- Function Generators
- Tone Controls
- Power Supplies
- Portable Instruments
- Intrusion Alarm Systems

Pinout



Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
CA3140AE	-55 to 125	8 Ld PDIP	E8.3
CA3140AEZ* (See Note)	-55 to 125	8 Ld PDIP (Pb-free)	E8.3
CA3140AM (3140A)	-55 to 125	8 Ld SOIC	M8.15
CA3140AM96 (3140A)	-55 to 125	8 Ld SOIC Tape and Reel	
CA3140AMZ (3140A) (See Note)	-55 to 125	8 Ld SOIC (Pb-free)	M8.15
CA3140AMZ96 (3140A) (See Note)	-55 to 125	8 Ld SOIC Tape and Reel (Pb-free)	
CA3140E	-55 to 125	8 Ld PDIP	E8.3
CA3140EZ* (See Note)	-55 to 125	8 Ld PDIP (Pb-free)	E8.3
CA3140M (3140)	-55 to 125	8 Ld SOIC	M8.15
CA3140M96 (3140)	-55 to 125	8 Ld SOIC Tape and Reel	
CA3140MZ (3140) (See Note)	-55 to 125	8 Ld SOIC (Pb-free)	M8.15
CA3140MZ96 (3140) (See Note)	-55 to 125	8 Ld SOIC Tape and Reel (Pb-free)	

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

CA3140, CA3140A

Absolute Maximum Ratings

DC Supply Voltage (Between V+ and V- Terminals) 36V
 Differential Mode Input Voltage 8V
 DC Input Voltage (V+ +8V) To (V- -0.5V)
 Input Terminal Current 1mA
 Output Short Circuit Duration ∞ (Note 2) Indefinite

Operating Conditions

Temperature Range -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W) θ_{JC} (°C/W)
 PDIP Package* 115 N/A
 SOIC Package 165 N/A
 Maximum Junction Temperature (Plastic Package) 150°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C
 (SOIC - Lead Tips Only)

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

- θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details
- Short circuit may be applied to ground or to either supply.

Electrical Specifications $V_{SUPPLY} = \pm 15V, T_A = 25^\circ C$

PARAMETER	SYMBOL	TEST CONDITIONS	TYPICAL VALUES		UNITS	
			CA3140	CA3140A		
Input Offset Voltage Adjustment Resistor		Typical Value of Resistor Between Terminals 4 and 5 or 4 and 1 to Adjust Max V_{IO}	4.7	18	k Ω	
Input Resistance	R_I		1.5	1.5	T Ω	
Input Capacitance	C_I		4	4	pF	
Output Resistance	R_O		60	60	Ω	
Equivalent Wideband Input Noise Voltage (See Figure 27)	e_N	BW = 140kHz, $R_S = 1M\Omega$	48	48	μV	
Equivalent Input Noise Voltage (See Figure 35)	e_N	$R_S = 100\Omega$	f = 1kHz	40	40	nV/ \sqrt{Hz}
			f = 10kHz	12	12	nV/ \sqrt{Hz}
Short Circuit Current to Opposite Supply	I_{OM+}		Source	40	40	mA
	I_{OM-}		Sink	18	18	mA
Gain-Bandwidth Product, (See Figures 6, 30)	f_T		4.5	4.5	MHz	
Slew Rate, (See Figure 31)	SR		9	9	V/ μs	
Sink Current From Terminal 8 To Terminal 4 to Swing Output Low			220	220	μA	
Transient Response (See Figure 28)	t_r	$R_L = 2k\Omega$ $C_L = 100pF$	Rise Time	0.08	0.08	μs
	OS		Overshoot	10	10	%
Settling Time at 10V _{P-P} , (See Figure 5)	t_S	$R_L = 2k\Omega$ $C_L = 100pF$ Voltage Follower	To 1mV	4.5	4.5	μs
			To 10mV	1.4	1.4	μs

Electrical Specifications For Equipment Design, at $V_{SUPPLY} = \pm 15V, T_A = 25^\circ C$, Unless Otherwise Specified

PARAMETER	SYMBOL	CA3140			CA3140A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$ V_{IO} $	-	5	15	-	2	5	mV
Input Offset Current	$ I_{IO} $	-	0.5	30	-	0.5	20	pA
Input Current	I_I	-	10	50	-	10	40	pA

CA3140, CA3140A

Electrical Specifications For Equipment Design, at $V_{SUPPLY} = \pm 15V$, $T_A = 25^\circ C$, Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	CA3140			CA3140A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Large Signal Voltage Gain (Note 3) (See Figures 6, 29)	A_{OL}	20	100	-	20	100	-	kV/V
		86	100	-	86	100	-	dB
Common Mode Rejection Ratio (See Figure 34)	CMRR	-	32	320	-	32	320	$\mu V/V$
		70	90	-	70	90	-	dB
Common Mode Input Voltage Range (See Figure 8)	V_{ICR}	-15	-15.5 to +12.5	11	-15	-15.5 to +12.5	12	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V_S$ (See Figure 36)	PSRR	-	100	150	-	100	150	$\mu V/V$
		76	80	-	76	80	-	dB
Max Output Voltage (Note 4) (See Figures 2, 8)	V_{OM+}	+12	13	-	+12	13	-	V
	V_{OM-}	-14	-14.4	-	-14	-14.4	-	V
Supply Current (See Figure 32)	I_+	-	4	6	-	4	6	mA
Device Dissipation	P_D	-	120	180	-	120	180	mW
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$	-	8	-	-	6	-	$\mu V/^\circ C$

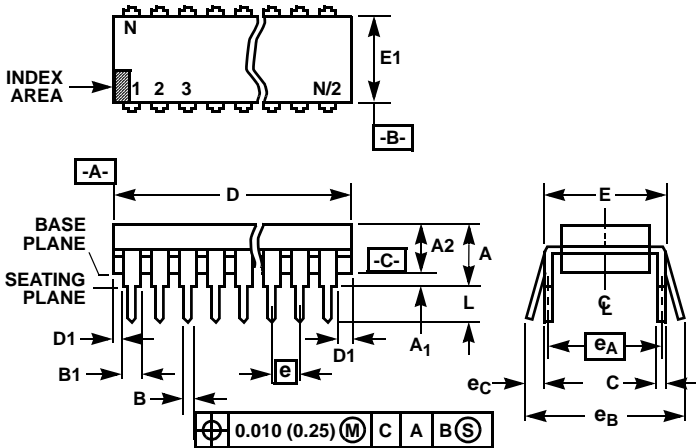
NOTES:

3. At $V_O = 26V_{P-P}$, +12V, -14V and $R_L = 2k\Omega$.
4. At $R_L = 2k\Omega$.

Electrical Specifications For Design Guidance At $V_+ = 5V$, $V_- = 0V$, $T_A = 25^\circ C$

PARAMETER	SYMBOL	TYPICAL VALUES		UNITS	
		CA3140	CA3140A		
Input Offset Voltage	$ V_{IO} $	5	2	mV	
Input Offset Current	$ I_{IO} $	0.1	0.1	pA	
Input Current	I_I	2	2	pA	
Input Resistance	R_I	1	1	$T\Omega$	
Large Signal Voltage Gain (See Figures 6, 29)	A_{OL}	100	100	kV/V	
		100	100	dB	
Common Mode Rejection Ratio	CMRR	32	32	$\mu V/V$	
		90	90	dB	
Common Mode Input Voltage Range (See Figure 8)	V_{ICR}	-0.5	-0.5	V	
		2.6	2.6	V	
Power Supply Rejection Ratio	PSRR $\Delta V_{IO}/\Delta V_S$	100	100	$\mu V/V$	
		80	80	dB	
Maximum Output Voltage (See Figures 2, 8)	V_{OM+}	3	3	V	
	V_{OM-}	0.13	0.13	V	
Maximum Output Current:	Source	I_{OM+}	10	10	mA
	Sink	I_{OM-}	1	1	mA
Slew Rate (See Figure 31)	SR	7	7	$V/\mu s$	
Gain-Bandwidth Product (See Figure 30)	f_T	3.7	3.7	MHz	
Supply Current (See Figure 32)	I_+	1.6	1.6	mA	
Device Dissipation	P_D	8	8	mW	
Sink Current from Terminal 8 to Terminal 4 to Swing Output Low		200	200	μA	

Dual-In-Line Plastic Packages (PDIP)



E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

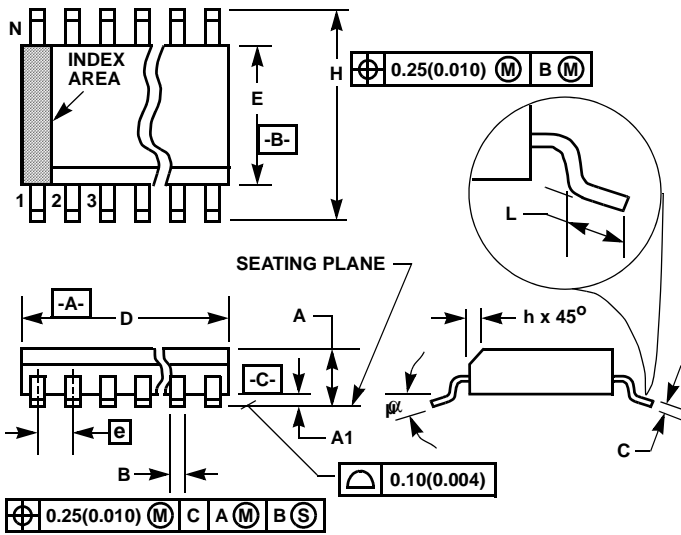
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		6
eB	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

NOTES:

- Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
- Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
- E and eA are measured with the leads constrained to be perpendicular to datum -C-.
- eB and eC are measured at the lead tips with the leads unconstrained. eC must be zero or greater.
- B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
- N is the maximum number of terminal positions.
- Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

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Small Outline Plastic Packages (SOIC)



M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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